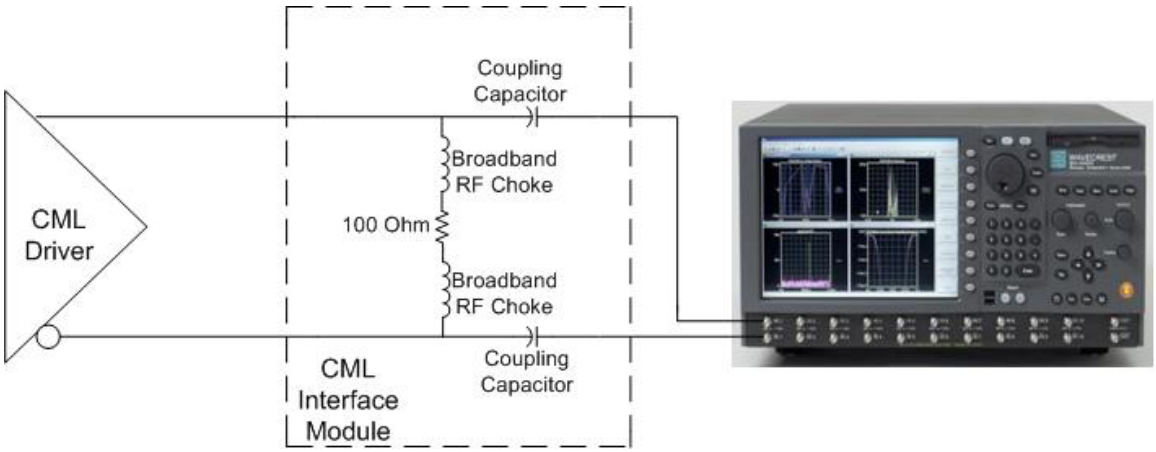
Product Description — CML Interface Module

Introduction

Current Mode Logic Interface Module - There are a number of low voltage signaling techniques in the market today that use current driven or current steering technology. However, current driven devices cannot be easily interfaced to ground based instruments because of DC bias requirements. *WAVECREST'S* CML Interface Module solves this problem by providing a true DC 100Ω differential termination that keeps CML device output stages properly biased while AC coupled to a ground-based instrument. An equivalent schematic of the device and its application appears below.



Operation - The CML Interface Module uses a broadband choking scheme that transfers the termination seen by a device from the 100Ω differential termination to a pair of 50Ω to ground terminations on the SIA-3000. At low frequencies, the 100Ω resistor provides a true differential termination for DC currents. At higher frequencies, the chokes open removing the resistor and AC coupling high-speed signals to the ground based differential terminations on an SIA-3000 channel card. The result is a high performance easy to use passive interface module for signal integrity measurements on CML devices.

Construction - The CML Interface module achieves excellent bandwidth by implementing several high-speed design techniques. The circuit layout is placed on a Roger's 4350 substrate that minimizes dielectric loss. The high bandwidth RF chokes tap the micro strip lines in a manner that minimizes parasitic capacitance. The CML Interface Module uses broadband SMA connectors that are spaced to easily mate with SIA-3000 channel cards as shown to the right.

Performance - The CML Interface was designed to provide controlled impedance beyond 5GHz. With three of the four ports terminated, the input impedance can be analyzed with an S_{11} measurement as shown in Figure 1. The return loss data below verifies that the chokes provide high impedance over 5 GHz, while the micro strip lines and coupling capacitor parasitics add little reactance to the real 50Ω load. The CML Interface Module is guaranteed to have a –3 dB insertion bandwidth of 6 GHz (see Figure 2) with a typical bandwidth of >7 GHz and a rise time of ~35ps.

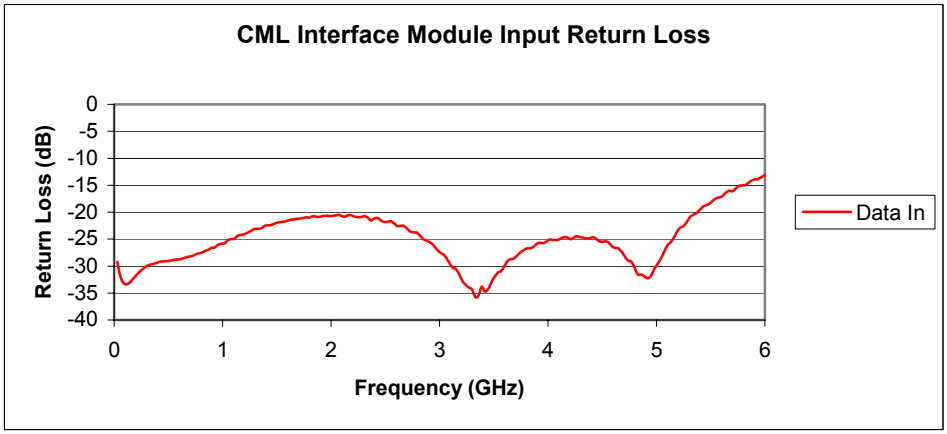


Figure 1

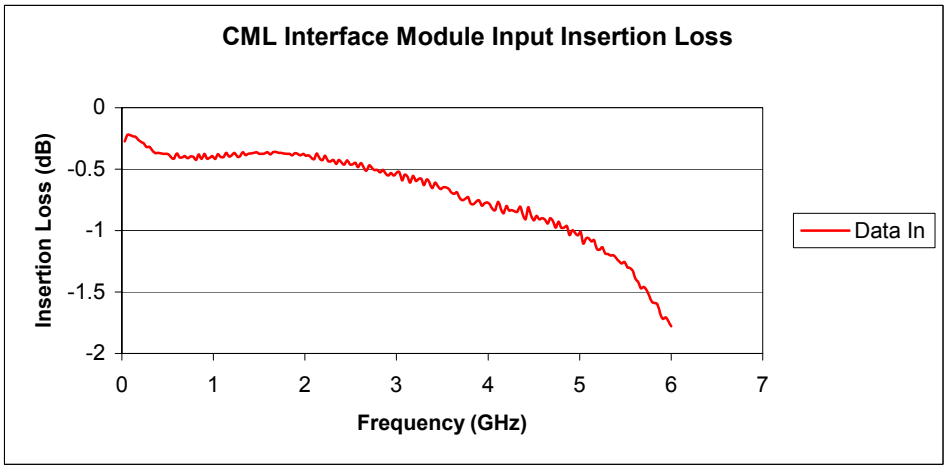


Figure 2